TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

The Applicant respectfully requests the Examiner to transfer FIGS. 1 – 3 from the file of the issued `043 patent to the reissue file.

In the Claims:

Please add the following new claims.

A1

24. A direct current sum bandgap voltage comparator comprising:

a summing node;

Sub B1

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor size in the first, second, and third current sources, respectively; and

and indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node.

25. A direct current sum bandgap voltage comparator comprising:

a summing node;

A1 cont.

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node, wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor size in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprises four current mirrors.

26. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant,

A1 cont.

and K_1, K_2, and K_3 are constants determined by a resistance and a transistor size in the first, second, and third current sources, respectively;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in a summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit of the logical signal indicates that the power supply voltage is equal to or greater than the predetermined threshold voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the predetermined threshold voltage.

27. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in the summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit if the logical signal indicates that the power supply voltage is equal to or greater than the preselected voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the preselected voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base

A1 cont.

emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor size in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprising four current mirrors.

28. A method, comprising:

generating a first current that changes with temperature according to a first polarity;

generating a second current that changes with temperature according to a second polarity; and

combining the first and second currents to generate a reference current.

Sub E1

29. The method of claim 28 wherein:

the first current changes with temperature according to a positive polarity; and

the second current changes with temperature according to a negative polarity.

30. The method of claim 28 wherein:

the first current is proportional to temperature; and

the second current is inversely proportional to temperature

31. The method of claim 28 wherein:

the first current increases as temperature increases and decreases as temperature decreases; and

the second current decreases as temperature increases and increases as temperature decreases.

32. The method of claim 28 wherein combining the first and second currents comprises summing the first and second currents.

33. The method of claim 28 wherein combining the first and second currents comprises sinking the first and second currents from a node.

A1 cont. Sub B2

34. The met[illegible] of claim 28 wherein combining th[illegible]t and second currents comprises sourcing the first and second currents to the node.

35. The method of claim 28, further comprising comparing the reference current to a current that is related to a power-supply voltage.

36. A method, comprising:

generating a first current that changes with temperature according to a first polarity;

generating a second current that changes with temperature according to a second polarity; and

combining the first and second currents at a node to generate a voltage on the node.

37. The method of claim 36 wherein combining the first and second currents comprises sourcing the first and second currents to the node.

38. The method of claim 36 wherein combining the first and second currents comprises sinking the first and second currents from the node.

39. The method of claim 36, further comprising comparing the voltage on the node to a reference voltage.

40. A method, comprising:

Sub C2

generating a first current that increases as temperature increases and that decreases as temperature decreases;

generating a second current that decreases as temperature increases and that increases as temperature decreases;

generating a third current that is related to a first voltage; and

combining the first, second, and third currents at a node to generate a second voltage on the node.

A1 cont.

41. The method of claim 40 wherein combining the currents comprises:

sinking the first and second currents from the node; and

sourcing the third current to the node.

Sub E7

42. The method of claim 40 wherein:

the first current is related to a thermal voltage; and

the second current is related to a voltage across a forward-biased p-n junction.

43. The method of claim 40 wherein:

the first current is related to a thermal voltage; and

the second current is related to a base-emitter voltage of a bipolar transistor.

44. The method of claim 40 wherein the second current is related to the natural logarithm of a current through a bipolar transistor.

45. A method, comprising:

Sub C3

generating a first current that is related to temperature according to a first polarity;

generating a second current that is related to temperature according to a second polarity;

combining the first and second currents into a reference current;

generating a third current; and

comparing the third current to the reference current.

46. The method of claim 45 wherein:

the first current is related to a thermal voltage;

the second current is related to a voltage across a forward-biased p-n junction; and

the third current is related to a power-supply voltage.

47. The method of claim 45 wherein:

combining the first and second currents comprises sinking the first and second currents from a node; and

comparing the third current to the reference current comprises,

A1 cont.

sourcing [illegible] third current to the node, and

comparing a voltage on the node to a reference voltage.

48. A method, comprising:

Sub B3

generating a first current that is proportional to a threshold voltage of a field-effect transistor;

generating a second current that is proportional to a difference between a supply voltage and a threshold voltage of a second field-effect transistor;

generating a third current that is proportional to a base-emitter voltage of a first bipolar transistor;

generating a fourth current that is proportional to the natural logarithm of a current through a second bipolar transistor; and

driving a node with the first, second, third, and fourth currents.

49. The method of claim 48 wherein driving the node comprises:

sourcing the first and second currents to the node; and

sinking the third and fourth currents from the node.

Sub E1

50. The method of claim 48, further comprising comparing a voltage on the node with a reference voltage.

51. The method of claim 48 wherein the first field-effect transistor is matched to the second field-effect transistor.

52. The method of claim 48 wherein the threshold voltage of the first field-effect transistor is equal or approximately equal to the threshold voltage of the second field-effect transistor.

53. A method, comprising:

generating a first current that equals a product of a first constant and a threshold voltage of a first field-effect transistor;

generating a second current that equals a product of a second constant and a difference between a supply voltage and a threshold voltage of a second field-effect transistor;